DINA MAHMOUD

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EDUCATION

Doctor of Philosophy in Computer and Communication Sciences| École Polytechnique Fédérale de Lausanne (EPFL) **Sep 2019 –**

- Relevant courses: Machine learning, Software security, Design technologies for integrated systems, Concurrent algorithms

Bachelor of Science in Electronics and Communications Engineering (ECNG) | The American University in Cairo (AUC) **Sep 2014 – Jan 2019**

- GPA: 3.989/4.0 (Dean's Honors List)
- Minor: Mathematics
- Relevant courses: Computer Organization and Assembly Language Programming, Digital Logic Design, Microcontroller System Design, VLSI

HONORS AND AWARDS

Cyber-Defense Campus Doctoral Fellowship| Sep 2020 -
Google Generation Scholarship| 2022
Ecole Doctorale d'Informatique et de Communication (EDIC) Fellowship| Sep 2019 – August 2020
Zewail Prize for Best Original Essay on a Multidisciplinary Topic| AUC, 2019
Academic Achievement Scholarship| AUC, 2014-2019
Highest GPA in the Senior Electronics and Communications Engineering Class | AUC, 2018
Outstanding Academic Achievers' Honors Assembly |AUC, 2017-2018
First Place in CSCE1101 (Programming Fundamentals) Programming Contest |AUC, 2015

TEACHING EXPERIENCE

Teaching Assistant | EDIC, EPFL, Fall 2020 – Fall 2022

- Responsible guiding and providing help to students through the labs and projects of the Computer Architecture I course.
- Guided students through weekly labs involving VHDL and assembly programming.

Head Teaching Assistant | EDIC, EPFL, Spring 2020 – Spring 2021

- Responsible for the programming part of the Information, Calcul, Commuincation (ICC) course.
- Guided students (300+) through weekly programming exercises in C (Spring 2020) and Python.
- Launched automated grading platform for students in C and Python courses.

Teaching Assistant | Dept. of ECNG, AUC, Spring 2019

- Guided students through execution of laboratory experiments for Digital Logic Design and Microcontroller System Design and helped them find causes of their errors by teaching them the troubleshooting approaches.
- Helped students with their assignments, course projects, and graduation projects.

Head Undergraduate Teaching Assistant | Dept. of ECNG, AUC, Fall 2016 – Spring 2017

- Clarified concepts to students and guided them in figuring out how to solve Digital Logic Design problems.
- Held review sessions for 20+ students.

RESEARCH EXPERIENCE

Doctoral Assistant | Parallel Systems Architecture (PARSA) Laboratory, EDIC, EPFL, Sep 2019 –

- Working on research topics targeting hardware security of heterogeneous FPGA-CPU-GPU systems.
- Publications:
  1. D. G. Mahmoud et al. "X-Attack 2.0: The Risk of Power Wasters and Satisfiability Don't-Care Hardware Trojans to Shared Cloud FPGAs," in IEEE Access, Jan. 2024.
  2. D. G. Mahmoud et al., "DFAulted: Analyzing and Exploiting CPU Software Faults Caused by FPGA-Driven Undervolting Attacks," in IEEE Access, Dec. 2022.
  3. D.G. Mahmoud et al., "FPGA-to-CPU Undervolting Attacks," Design, Automation & Test in Europe (DATE), Antwerp, Belgium, Mar. 2022.
  4. D. G. Mahmoud et al., "Electrical-Level Attacks on CPUs, FPGAs, and GPUs: Survey and Implications in the Heterogeneous Era," ACM Computing Surveys, 2022.
  5. O. Glamocanin et al., "Shared FPGAs and the Holy Grail: Protections against Side-Channel and Fault Attacks," in Design, Automation & Test in Europe (DATE), 2021.

6. Demonstrating a new attack vector on shared FPGAs: D. G. Mahmoud et al., "X-attack: Remote Activation of Satisfiability Don't-Care Hardware Trojans on Shared FPGAs," paper presented at the 30th International Conference on Field-Programmable Logic and Applications (FPL), 2020.

Research Assistant | SEAD Group, AUC **Jan 2017 – Aug 2019**

- Worked on research topics related to fault tolerance and simulation of digital and mixed circuits.
- Publications:
  1. D.G. Mahmoud et al., "Runtime Replacement of Machine Learning Modules in FPGA-Based Systems," Proc. of 10th Mediterranean Conference on Embedded Computing (MECO), Budva, Montenegro, 2021.
  2. B. Shokry et al., "Triple Event Upset Tolerant Area-Efficient FPGA-Based System for Space Applications And Nuclear Plants," in Proc. of 16th IEEE International Conference on Factory Communication Systems (WFCS), Porto, 2020.
  3. Increasing the reliability of chip-to-chip interconnections in the automotive industry: M.G. Labib et al., "Heterogeneous Redundancy for PCB Track Failures: An Automotive Example," in Proc. of 14th International Conference on Computer Engineering and Systems (ICCES), Cairo, 2019.
  4. Proposing a more reliable architecture for on-chip memory for FPGA critical systems: M. Rumman et al., "Reliable On-Chip Memory For FPGA-Based Systems," in 31st IEEE Intl. Conf. on Microelectronics (ICM), Cairo, 2019.
  5. G. I. Alkady et al., "Reliable FPGA-Based Network Architecture for Smart Cities," in Proc. of 31st IEEE Intl. Conf. on Microelectronics (ICM), Cairo, 2019.
  6. Studying the possibility of using Ethernet networks in a state-of-the-art production line with high-sampling-rate machines while meeting the critical deadlines of the system and providing fault tolerance: A. Gabara et al., "Fault-Tolerant High-Rate Ethernet-Based Networked Control System," in IEEE Intl. Novel Intelligent and Leading Emerging Sciences Conf. (NILES), Cairo, 2019, pp. 84–87.
  7. Proposing an FPGA-based system for monitoring students' focus to enhance educational programs: M. Hanna et al., "Smart FPGA-based System for Enhancing Educational Programs," in IEEE Intl. Novel Intelligent and Leading Emerging Sciences Conf. (NILES), Cairo, 2019, pp. 122–125.
  8. Proposing an implementation for the Triple Modular Redundancy digital voter to guarantee either correct output or error signaling: D. G. Mahmoud et al., "Fault secure FPGA-based TMR voter," in 7th IEEE Mediterranean Conf. on Embedded Computing (MECO), Budva, 2018, pp. 1–4.
  9. M. Y. ElSalamouny et al., "Highly available FPGA-based smart band for WBAN," in 12th IEEE Intl. Conf. on Computer Engineering and Systems (ICCES), Cairo, 2017, pp. 25–30.

Summer@EPFL Research Intern | Parallel Systems Architecture Laboratory, EPFL, Jun – Aug 2018

- Accepted to the Summer Research program (acceptance rate in 2018 was 1.9%).
- Published a research paper showing the feasibility of a fault attack using power waster circuits on Xilinx FPGA, paving the way for more research in the area: D. Mahmoud and M. Stojilovic, "Timing Violation Induced Faults in Multi-Tenant FPGAs," in Design, Automation & Test in Europe (DATE), Florence, Italy, Mar. 2019, pp. 1745–1750.

Bachelor's Graduation Project | AUC **Feb – Dec 2018**

- Explored power management techniques for electric vehicles and implemented driving cycle classification using NN Toolbox in MATLAB. Developed a HW prototype using Arduino microcontroller and Zynq board.
- Publication: D. G. Mahmoud et al., "Intelligent Battery-Aware Energy Management System for Electric Vehicles," in 24th IEEE Intl. Conf. on Emerging Technologies and Factory Automation (ETFA), Zaragoza, Spain, 2019, pp. 1635–1638.

PROFESSIONAL ACTIVITIES

Member, Technical Program Committee, IEEE International Conference on Emerging Technologies and Factory Automation (ETFA), 2021

Student Member, ACM SIGARCH, WiCARCH, IEEE

EXTRACURRICULAR ACTIVITIES

Mentor and Speaker, Coding Club des Filles, September 2021 -

- Mentoring school girls on Dacodeck.ch to help them with their coding journey and to answer their questions.
- Spoke to school girls about my professional journey and introduced them to the basics of logic circuits and their security.

Hopper, Virtual Grace Hopper Celebration (vGHC), 2021

- Volunteered to help run vGHC, providing session reviews and acting as a professional viewer.

Speaker, Toi aussi, crée ton appli, Summer 2021

- Introduced 21 girls aged 12 to 16 to the basics of logic circuits and their security.

Student Representative, Research and Creativity Convention (RCC) Organizing Committee, Fall 2018

- Represented the entire student body of 5,474 undergraduate students.
- Helped in organizing the Research and Creativity Convention 2019 and contributed to promoting it to students.

Member and Copilot, Robotics AUC ROV team, Jan 2017 – Aug 2017

- Contributed to building the control system of a remotely operated vehicle (ROV) and chosen by the team of 21 members (48% female) to act as copilot during the regional competition. Won 7th place among 19 entries.

Intermediate Program Head, Robotics Club, AUC, Jul 2016 – May 2017

- Responsible for quality and content of the newly established intermediate program.
- Organized meetings with the technical heads (20% female) and sessions with the members.

Physics Team Head, Egyptian Researchers, Mar – Sep 2016

- Wrote articles on topics in Physics to be published on Facebook and edited the team members' articles.
- Organized the article timing and content for the team.

Basic Technical Head, Robotics Club, AUC, Fall 2015 – Spring 2016

- Taught new members basics of Arduino programming and connecting digital circuits.

INTERNSHIPS

Intern | Electrical Systems Engineering Company (ESEC) **Jul – Aug 2017**

- Responsible for troubleshooting and repairing devices (digital low resistance ohmmeters and power analyzers) by interpreting circuits' diagrams and tracing faults using multimeters.

Trainee | Engineering for the Petroleum and Process Industries (ENPPI) **Jul 2017**

- Trained in the Instrumentation Engineering and Telecommunications Systems departments.

ACADEMIC PROJECTS

Google EMEA Get Ahead Program, Summer 2021.

- Solved weekly coding assignments and participated in the Google coding challenge.

Machine Learning for Side-Channel Disassembly, Machine Learning, Fall 2020.

- Implemented neural networks to identify processor instructions executed and their operands based on the electromagnetic (EM) emanation measurements of a RISC-V processor.
- Used keras and tsaug libraries.

Implementation and Optimization of a FIR Filter, Design Technologies for Integrated Systems, Fall 2019.

- Optimized the design of a 10-stage FIR filter.
- Used ModelSim and Synopsys Design Compiler to test the optimized design.

Channel Coding for a Wimax System, ASIC, Spring 2018.

- Implemented the channel coding (QPSK) for Wimax on an FPGA, using Altera Quartus and ModelSim.

Smart Home Control, Power and Machines, Spring 2018.

- Programmed an Arduino with a Wi-Fi module to remotely control LEDs and a DC motor, using Blynk application.

4-bit Low Power ALU, VLSI, Fall 2017.

- Designed a power optimized 4-bit ALU. Implemented with PTL and CMOS logic in 0.18um technology node.

Performance Evaluation 16-QAM, QPSK, and Huffman Encoding, Digital Communications, Fall 2017.

- Simulated the performance of QPSK and 16 QAM over AWGN channel, and Huffman encoding using MATLAB.

An Airplane Boarding System, Microcontroller Design, Fall 2017.

- Implemented using a microcontroller, an Ethernet shield, LCD, keypad, H-bridge, DC motor, and Ultrasonic sensor.

Traffic Lights Control System, Automatic Control, Fall 2017.

- Designed the system using optocouplers, pushbuttons, LEDs, timers, and Arduino microcontroller.

Implementation of an Optical Communication System, Analog Circuits, Spring 2017.

- Designed and implemented on a PCB an optical communication system.

ARM Thumb Simulator, and Cache Performance Evaluation, Computer Organization, Summer 2016.

- Implemented an ARM thumb in C++. Evaluated cache memory performance w.r.t. various replacement policies.

Implementation of a Game using SFML, Programming Fundamentals, Fall 2015.

- Implemented a game with its graphical user interface using SFML and C++ programming language.

SKILLS

- Arabic: native
- English: C1
- French: B2
- German: A1
- Chinese: beginner

- Good knowledge of C/C++, Python, Verilog, SystemVerilog and VHDL.
- Basic knowledge of Git, Bash, Java, and HTML5.
- Competent user of Linux, Microsoft Visual Studio Code, Matlab, Cadence, ModelSim, Intel Quartus, Xilinx Vivado, Xilinx SDK, and Arduino.
- Novice user of Eldo, Questa ADMS, Riverbed, and Wireshark.

References furnished upon request